IN THE CLAIMS:

Please amend the claims as set forth below:

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1. (Currently Amended) A processor comprising:

a register configured to store a first number of bits; and

an execution core coupled to said register, wherein said execution core is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to ~~selectively~~ zero extend said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number.

2. (Original) The processor as recited in claim 1 wherein said result comprises a number of bits specified by said operand size.

3-7. (Cancelled)

8. (Currently Amended) The processor as recited in claim 1 wherein said execution core is coupled to receive an operating mode of said processor, and wherein said execution core is configured to ~~selectively~~ zero extend said result further responsive to said operating mode.

9. (Currently Amended) The processor as recited in claim 8 wherein said operating mode includes a default operand size, and wherein said operand size corresponding to said instruction is said default operand size unless overridden by an encoding of said

instruction. ~~instruction's encoding~~.

10. (Original) The processor as recited in claim 9 wherein said execution core is configured to zero extend said result if said operand size is said default operand size.

11. (Currently Amended) The processor as recited in claim 9 wherein said default operand size is overridden by said ~~instruction's~~ encoding if said instruction includes one or more operand size override prefixes.

12. (Cancelled)

13. (Currently Amended) A computer-implemented method comprising:

executing an instruction to produce a result, said instruction having a register as a destination and said register configured to store a first number of bits; ~~and~~

~~selectively~~ zero extending said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits; and

preserving a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number.

14. (Original) The method as recited in claim 13 wherein said result comprises a number of bits specified by said operand size.

15-16. (Cancelled)

17. (Currently Amended) The method as recited in claim 13 wherein said ~~selectively~~

zero extending and said preserving are further ~~is further~~ responsive to an operating mode of a processor performing said executing.

18. (Currently Amended) The method as recited in claim 17 wherein said operating mode includes a default operand size, ~~wherein said selectively zero extending~~ and the method further comprises zero extending said result if said operand size is said default operand size.

19. (Cancelled)

20. (New) An apparatus comprising:

a storage location corresponding to a register, said register defined to store a first number of bits; and

an execution circuit coupled to said storage location, wherein said execution circuit is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to zero extend said result for update in said storage location responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution circuit is configured to preserve a value of at least a portion of said bits in said storage location that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number.

21. (New) The apparatus as recited in claim 20 wherein said result comprises a number of bits specified by said operand size.

22. (New) The apparatus as recited in claim 20 wherein said execution circuit is coupled

to receive an operating mode, and wherein said execution circuit is configured to zero extend said result further responsive to said operating mode.

B1 23. (New) The apparatus as recited in claim 22 wherein said operating mode includes a default operand size, and wherein said operand size corresponding to said instruction is said default operand size unless overridden by an encoding of said instruction.

24. (New) The apparatus as recited in claim 23 wherein said execution circuit is configured to zero extend said result if said operand size is said default operand size.

25. (New) The apparatus as recited in claim 23 wherein said default operand size is overridden by said encoding if said instruction includes one or more operand size override prefixes.

26. (New) An apparatus comprising:

a storage location corresponding to a register, said register defined to store a first number of bits; and

an execution circuit ~~co~~upled to said storage location, wherein said execution circuit is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to extend said result to said first number of bits for update in said storage location responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution circuit is configured to preserve a value of at least a portion of said bits in said storage location that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number.

27. (New) The apparatus as recited in claim 26 wherein said result comprises a number of bits specified by said operand size.

28. (New) The apparatus as recited in claim 26 wherein said execution circuit is coupled to receive an operating mode, and wherein said execution circuit is configured to selectively extend said result further responsive to said operating mode.

29. (New) The apparatus as recited in claim 28 wherein said operating mode includes a default operand size, and wherein said operand size corresponding to said instruction is said default operand size unless overridden by an encoding of said instruction.

30. (New) The apparatus as recited in claim 29 wherein said execution circuit is configured to extend said result to said first number of bits if said operand size is said default operand size.

31. (New) The apparatus as recited in claim 29 wherein said default operand size is overridden by said encoding if said instruction includes one or more operand size override prefixes.

32. (New) A computer system comprising:

a processor comprising a register configured to store a first number of bits and an execution core coupled to said register, wherein said execution core is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to zero extend said result for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first

number of bits and different from said second number; and

an input/output (I/O) device configured to communicate between said computer system and another computer system.

24 33. (New) The computer system as recited in claim 23 wherein the I/O device comprises a modem.

25 34. (New) The computer system as recited in claim 23 further comprising an audio device.

26 35. (New) A computer system comprising:

a processor comprising a register configured to store a first number of bits and an execution core coupled to said register, wherein said execution core is configured to execute an instruction to produce a result, said instruction having said register as a destination, and wherein said execution core is configured to extend said result to said first number of bits for update in said register responsive to an operand size corresponding to said instruction specifying a second number of bits less than said first number of bits, and wherein said execution core is configured to preserve a value of at least a portion of said bits in said register that are not updated by said result responsive to said operand size specifying a third number of bits less than said first number of bits and different from said second number; and

an input/output (I/O) device configured to communicate between said computer system and another computer system.

27 36. (New) The computer system as recited in claim 35 wherein the I/O device comprises a modem.

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37. (New) The computer system as recited in claim 35 further comprising an audio device.